Introduction.

A couple years ago I set out to create a RAM expansion for my 9835A. Using the schematic of the HP RAM card I created and observing the memory bus using a logic analyzer I came up with a design that appear to work, but I had suspicions that all was not good. Earlier this year I was loaned a diagnostic RAM and ROM module, and the diagnostics confirmed my suspicions, the card would randomly fail the byte wide tests. I then set about dumping the contents of the diagnostic ROM and creating a duplicate of the diagnostic RAM. Along the way I got side tracked by some other things, but last week I managed to create a working duplicate of the diagnostic RAM, and made my work available to the community and then turned my attention back to my RAM card. I had noted that the HP memory card latched the state of the -BYTE signal, but from what observed using my logic analyzer this did not seem necessary as it appeared -BYTE persisted through the entire cycle, so I thought I must have a timeing issue and I proceeded to make some adjustments to signal timing but the card failed the same way. I then proceeded to alter some of the logic in the BLKSEL2 PLD so that the state of -BYTE and -BL would be effectively latched at the beginning of the memory cycle and that resolved the problem. The RAM diagnostics ran clean on all eight expansion blocks of RAM, I then started the memory exerciser, what the service guide says is a more thorough test, and went to bed. When I stopped the test the next afternoon it had completed on the base memory and 2 blocks of my expansion card. I noted when it started and completed the last block and found it takes nearly 6 hour for this test to complete on one 64K byte block, to run this test on all of the memory would have taken days.

The 9835 Memory Bus

The processor used in the 9835 is a 16 bit processor that in its original versions could address 32K Words of memory. The version that is used in the 9835 had a bank selection scheme built into the processor that allowed it to address up to 65,535 banks of 32K words each by providing some 16bit bank selection registers, the bit from the active bank select register are brought out on block select pins, however in the case of the 9835 only 7 of them are connected to the memory bus so that limits the machine to 128 blocks of which the even block numbers are used for RAM and the odd blocks are used for ROM with the exception of block 1 which is used by the virtual PPU processor. So that leaves us with a maximum of 64 64K blocks of memory or 4MB of memory, which is probably still beyond the wildest dreams of the systems designers, with the memory technology available at the time the system maxed out at 256K of RAM.

Some of the important signals on the memory bus:

IDA0-15	This is a multiplexed, 16 bit, active low address and data bus only 15 of the 16 bits are actually used to address memory.
BSC0-6	Active low block select signals
RAL	The processor's registers are mapped over the bottom 37 addresses om each block of memory. RAL is used to inhibit external memory during register accesses.
BYTE	Active low signal that indicate that the current cycle is for a single byte.
BL	Active low signal that indicates which byte in the addressed word is the target BL=Byte Left when low the target is the Left or MSB. It is only important for writes when you want to be sure you update the correct byte on reads the CPU knows which byte it wants and picks it off.
PH2_TTL	Phase 2 of the two phase CPU clock basic timing signal
RAMALE	HP calls this signal STM it is an active low signal that indicates that a valid address is present on the bus indicating the start of a bus cycle
SMC	Synchronous Memory Complete on read cycles this signal goes high to in response to receiving UMC from the memory device and is used to gate the data onto the memory bus.
UMC	Unsynchronized Memory complete this is a handshake signal used by the memory to acknowledge that it is ready to continue with the memory cycle, delaying UMC will lengthen the cycle. While drawing schematics of the CPU card I discovered that there is another signal on the memory bus that when pulled low will inhibit UMC pin 38 I have labeled it -Wait
WRT	Active low signal indicating that the cycle is a write cycle.

My Card.

This card is only useful as expansion memory it cannot be used for base memory because on the 9835 a portion of the base memory card is mapped off and used as base page memory for the 9835's virtual PPU. I chose to use SRAM since interfacing SRAM is easier and large fast SRAMs are available cheaply. For my card I used four M5M510008 55nS 128K x 8 chips. Each pair of SRAMs provides four blocks of memory expansion allowing the 9835 to be expanded beyond what would have been available originally. These SRAMs are much faster than required, but I used them because I had them already. A pair of 74LS374 registers latch the address, and a pair of 74LS245 transceivers interface the data pins to the bus.

The address decoding is done by a PALCE22V10, a GAL 22V10 could also be used. This PLD has for inputs BSC0-6, RAL, BYTE, and BL. The combination of these inputs is used to generate the appropriate chip select signals for SRAM chips and also the top two bit of the address for the RAM chips. It also outputs a signal that indicates memory on the card is being addressed. All of the input signals are stable at the time that ALE drops and the outputs are latched at that time. Since these PLDs latch registered outputs on the rising edge, it is clocked by an inverted ALE signal. Included in the package with this document is BLKSEL2.PDS which is the text input file to PALASM to generate the PLD.

There is a second PLD on this card a PALCE16V8 and again a GAL16V8 could be used in its place. This PLD is mostly some miscellaneous glue logic for the card. It has 3 registered outputs that are only used internally in the PLD for sequencing. The PLD is clocked by the phase 2 clock on the bus. On the first rise of PH2 after the SELECTED signal from from the BLKSEL2, approximately 52nS, CLK1 becomes active this activates UMC (RAW40) and also enables the 74LS245s. Approximately 150nS later on the next rise of PH2, CLK2 becomes active and on a write cycle the write signal to the RAM chips drops and remains low until CLK3 goes active 150nS later on the next rise of PH2. The SRAM chips I am using latch write data on on the rise of the -WE input, which I think is pretty common, so I thought it best to terminate the write signal before the end of the memory cycle but having it active for 150nS should be adequate for even the slowest memory in all from the drop of ALE the memory cycle is about 400-450nS long so my 55nS SRAM are way overkill. On read cycles, when SMC goes active in response to our card activating UMC, the SRAM outputs are enabled putting the contents of the addressed word onto the bus.

The remaining chip on the card is a 74LS125 tri-state buffer. Its main reason for being there is to activate the UMC signal. This signal is a wired OR so you cannot use a totem pole output TTL device to drive it, using one gate of a 74LS125 with the input tied low pulls the line low when we want to activate it and is otherwise in high impedence state. An open collector output device could also be used for this. The other three gates are used to buffer some signals on the card.

My Schematic.

Included in this package is a schematic of the card that I built. For simplicty I have only shown one pair of SRAMs on the schematic. The address lines, data lines, output enable and write enable lines are all wired the same way. The -CE2_H and -CE2_L signals are used to enable the SRAMs in the second pair. For all of the bus signals, the number in parenthesis is the pin number on the 50 pin memory bus connector.

Package Contents.

This document RAM_Card.pdf

Card schematic RAM_Schematic.pdf

PALASM source for BLKSEL2 PLD BLKSEL2.PDS

PALASM source for RAMMISC2 PLD RAMMISC2.PDS