Worldwide Response Center

HP 3000 APPLICATION NOTE #58

HPPA PATHING CONVENTIONS FOR HP3000 900 SERIES PROCESSORS (UPDATE)

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RESPONSE CENTER APPLICATION NOTES

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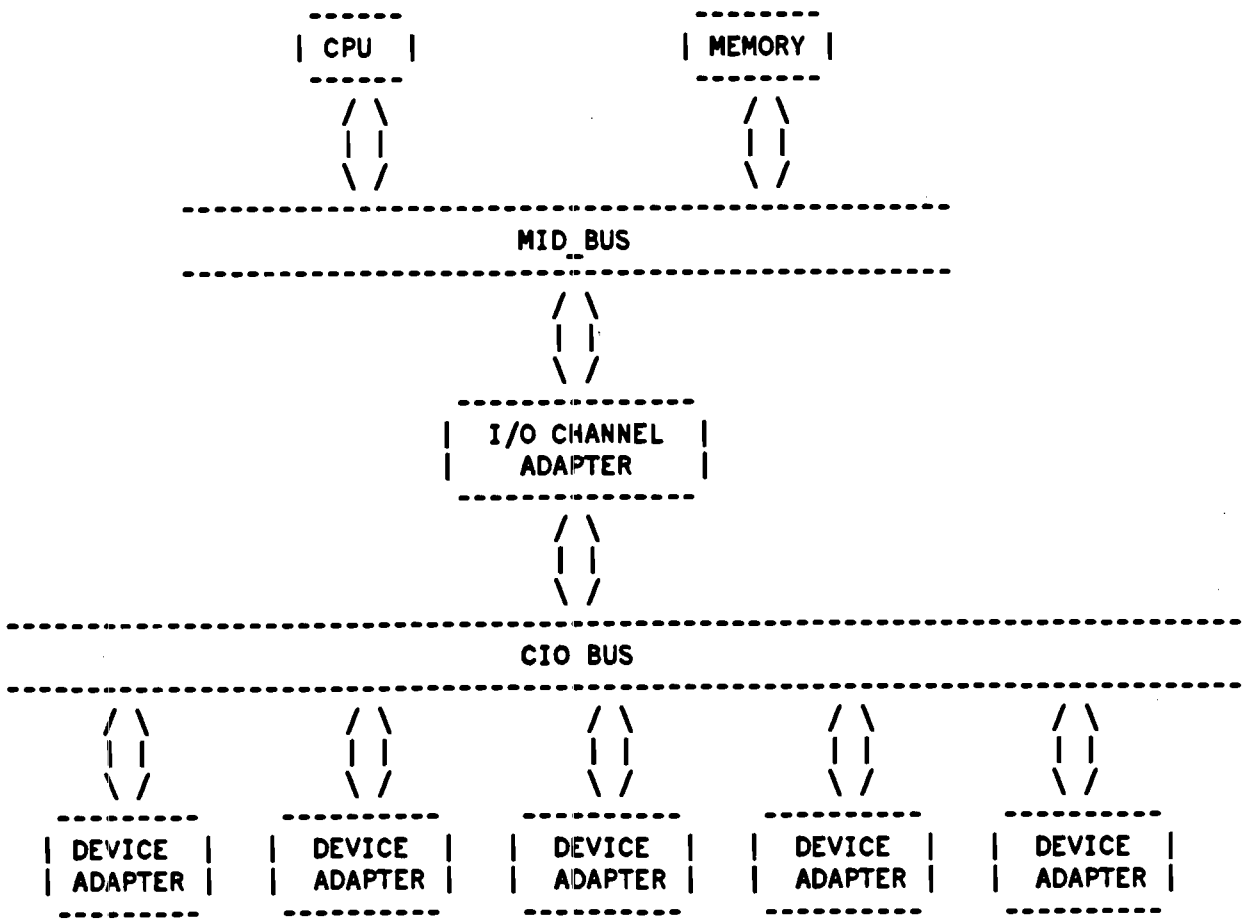
HPPA PATHING CONVENTIONS FOR HP3000 900 SERIES PROCESSORS

With the introduction of the new HPPA series of CPUs many things have changed, not the least of which is the new convention used in addressing I/O devices. Instead of the old formulas used on the "Classic 3000s (e.g. 128*IMB#+8*Channel#+Device#=DRT#), we now have to deal with new terminology and hardware concepts. This document will attempt to explain and identify these new terms and provide an overview of the hardware involved in performing "HPPA I/O". It will not be detailed, but will be enough to allow someone who is familiar with the Classic 3000 I/O system to understand the HPPA system. The end result should be that the reader will be able to understand the accompanying HPPA CPU backplane layouts and the associated "paths" for our current HP3000/9XX CPUs.

THE HP3000 SERIES 930

The Series 930 SPU was HP's first commercial HPPA system. It employed a discrete CPU and I/O hardware design and performed at 4.2 HPPA MIPS. The I/O on this machine, as well as on the 925 and 950, is performed using HP's CIO (Channel I/O) standard. This standard defines a processor- independent I/O channel which is usually connected to a high speed central bus (Mid_Bus) by what is called a Channel Adapter. The "channel" itself (CIO Bus) is usually a printed circuit I/O backplane and provides a communication path between a Channel Adapter (CA) and up to sixteen "Device Adapters" (DAs). These Device Adapters are the main I/O cards and have names like "HPIB Device Adapters" (similar to GICS), 802.3 LAN Device Adapters (similar to LANICS), 6-Channel MUXs (similar to ADCCs), etc. For purposes of illustration, the whole setup looks something like this...



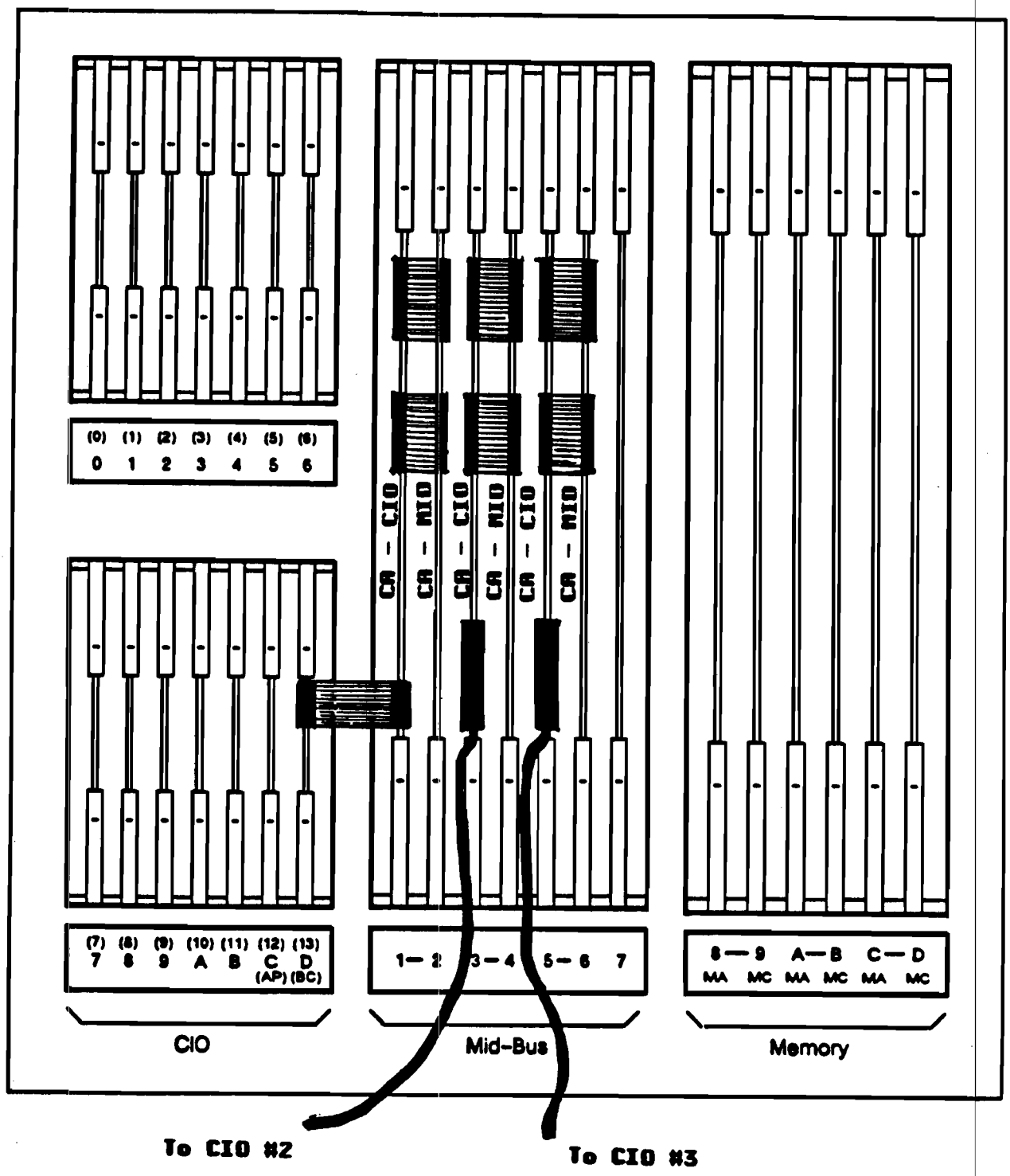
Well, you might be thinking "What does this mean to me?". In HPPA I/O configuration there is no equivalent to the "DRT". Instead, you must specify the "path" that leads from the Mid_Bus through the appropriate I/O Channel Adapter to its attached CIO Bus, through the appropriate Device Adapter and out to the appropriate device connected to the Device Adapter.

For the 930 CPU, the I/O channel is very similar to the above generic diagram. Its Mid_Bus is a single high speed bus connecting the CPU, Main Memory and I/O system(s) together. Since, in this implementation, there is only one Mid_Bus, its path does not have to be defined. Thus, you only have to describe the path from the I/O Channel Adapter to the actual peripheral device (e.g disc drive, printer or tape drive). A generic path descriptor would look like this...

I/O Channel Adapter # . Device Adapter # . Device #

The Series 930 may have up to three independent CIO Busses attached to the Mid_Bus via three Channel Adapters. Accordingly, the Channel Adapter number is equal to one of three values: 8, 16 or 24. The value assigned to any particular Channel Adapter is dependent upon the Mid_Bus slot position it is plugged into (more on this later). The Device Adapter number is equal to the slot position of the CIO Bus that the Device Adapter card is plugged into. Finally, the Device number is needed when you are working with a Device Adapter that can drive more than one external peripheral device. A good example of this is the HPIB Device Adapter, which is very similar to a GIC on the classic HP 3000. It supplies an HPIB Bus for HPIB-equipped peripherals. Since you can attach up to eight peripherals to any single HPIB Bus, each one requires a unique address. Thus, each HPIB-equipped peripheral is provided with a mechanism to supply an address and it is this address you use for the "Device #" in the formula above. Remember, for those Device Adapters that do not drive multiple external devices (e.g. 802.3 LAN Device Adapters) a Device # is not needed or desired and the path descriptor will end at the Device Adapter #.

In an attempt to clarify all this, we will now take a look at an actual 930 card cage/backplane layout and show how all these numbers are derived. As the diagram which follows shows, the I/O backplane on the 930 contains all the Channel Adapter card "sets" as well as the main CIO Bus (the other CIO Busses are located in an I/O Expander bay attached to the Channel Adapters via interconnecting cables). As stated previously, In the HP3000 Series 930 main CPU card cage, there are only two busses to deal with. A Mid_Bus with slots labeled "1" thru "D" and the 1st CIO Bus with slots "0" thru "D". To date, all of the CIO interface cards are 1/2 the height of the other CPU boards and, thus, CIO busses are easy to discriminate from all the other ones. It is important to note that one CIO slot is utilized as a dedicated interconnection to the appropriate Channel Adapter through a "CIO Buffer card" and that the Channel Adapter is actually a two board interconnected set within the Mid_Bus.



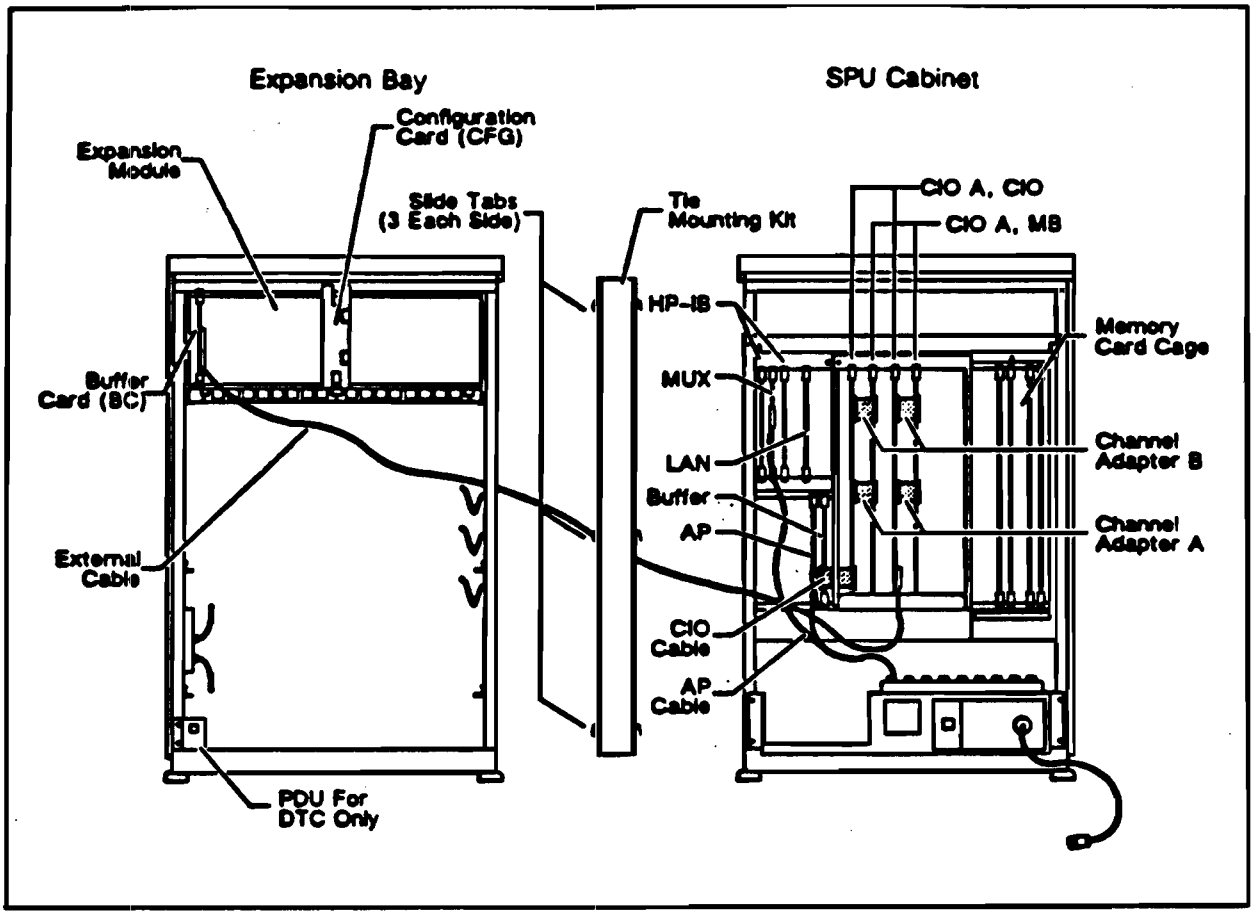
HP-930 Rear Card Cage Card Assignments

It isn't necessary to look at the actual hardware layout to figure out a path descriptor, but it can help in understanding how they are actually derived. For example, as previously described, the first path descriptor "element" is the I/O Channel Adapter # which, for a Series 930 system, can be either 8, 16, or 24. These numbers are actually derived by the generic formula that states "the Channel Adapter # is equal to 4 times the Mid_Bus slot # the Channel Adapter is plugged into". Since, in the 930 implementation, the Channel Adapters are two board sets, the 2nd card (called the CA MID) is the one used in the calculation of the Channel #. It will always occupy slots 2, 4 or 6 in the Mid_Bus and by multiplying these numbers by 4 we get 8, 16 or 24 as the Channel Adapter #.

The calculation of the Device Adapter # is somewhat easier since it is by definition equal to the number of the slot the Device Adapter of interest is plugged into. Thus, for an HPIB Device Adapter in slot 0 of the 1st CIO Bus, the path is 8.0 and for one in slot 0 of the 2nd CIO Bus it is 16.0 etc. Finally, the third element of the path descriptor, the Device #, is equal to the HPIB device number assigned to the disc, printer, tape drive, or whatever, is connected to the HPIB Device Adapter in question. Again, some Device Adapters do not provide the Device # functionality and as a result, their paths are only two elements long.

As previously stated, the HP3000 Series 930 may have up to 3 CIO Busses and two of them are located in an I/O expander card cage housed in a separate bay. The I/O expander bay is a standard feature of the Series 930 and is capable of being configured as either a single 16-slot CIO Bus or two 8-slot Busses. As of this writing, the only supported Series 930 configuration is the one with two independent 8-slot CIO Busses. Also standard on the Series 930 are two Channel Adapters. The third one can be ordered as an optional addition and will provide connectivity to the second half of the I/O expander.

To determine how to derive the path for a Device Adapter plugged into the expander, let's look at the example of an expander backplane configured for two 8-slot CIO Busses. Notice, although there are actually 20 slots in the backplane, four of them are reserved for special purposes. Of these, a CIO Buffer card plugs into slot "B1" and effectively connects Channel Adapter #2 (Mid_Bus module 16) to the first CIO Bus, slots 0 thru 7. A third Channel Adapter can be optionally connected to another CIO Buffer card in slot "B2" and addressed as Mid_Bus module 24. This will provide connectivity to slots 8 thru 15 of CIO Bus #3. The other two "special" slots - "A1" and "A2" - are used in conjunction with a "configuration" card which determines whether the I/O expander acts as a single 16-slot CIO Bus or two independent 8-slot CIO Busses. On the 930 Series, it will always be plugged into slot "A1" and configure the expander as two 8-slot CIO Busses. In this configuration, the addresses of Device Adapters inserted into slots 0 thru 7 will be 16.0 thru 16.7 while those in slots 8 thru 15 will be addressed as 24.0 (slot 8) thru 24.7 (slot 15). The addresses of any attached peripherals would follow as "Device #" descriptor elements as before.



Example: Two 8 Slot Installation

Peripherals	DA's Required
24 Disc Units	6
2 Tape Units + 2 Printers	2
200 Terminals	1
Network Services	1

0	1	2	3	4	5	6
DISC 1	MUX	DTCLAN				
7	8	9	10	11	12	13
					AP	BUFF 1

Main Bay CIO #1

B1	0	1	2	3	4	5	6	7	A1	A2	B2	8	9	10	11	12	13	14	15
BUFF 2	DISC 3	DISC 4	NSLAN	TAPE					CONFIG		BUFF 3	DISC 5	DISC 6	DISC	TAPE/PRNTR				

CIO #2 CIO #3

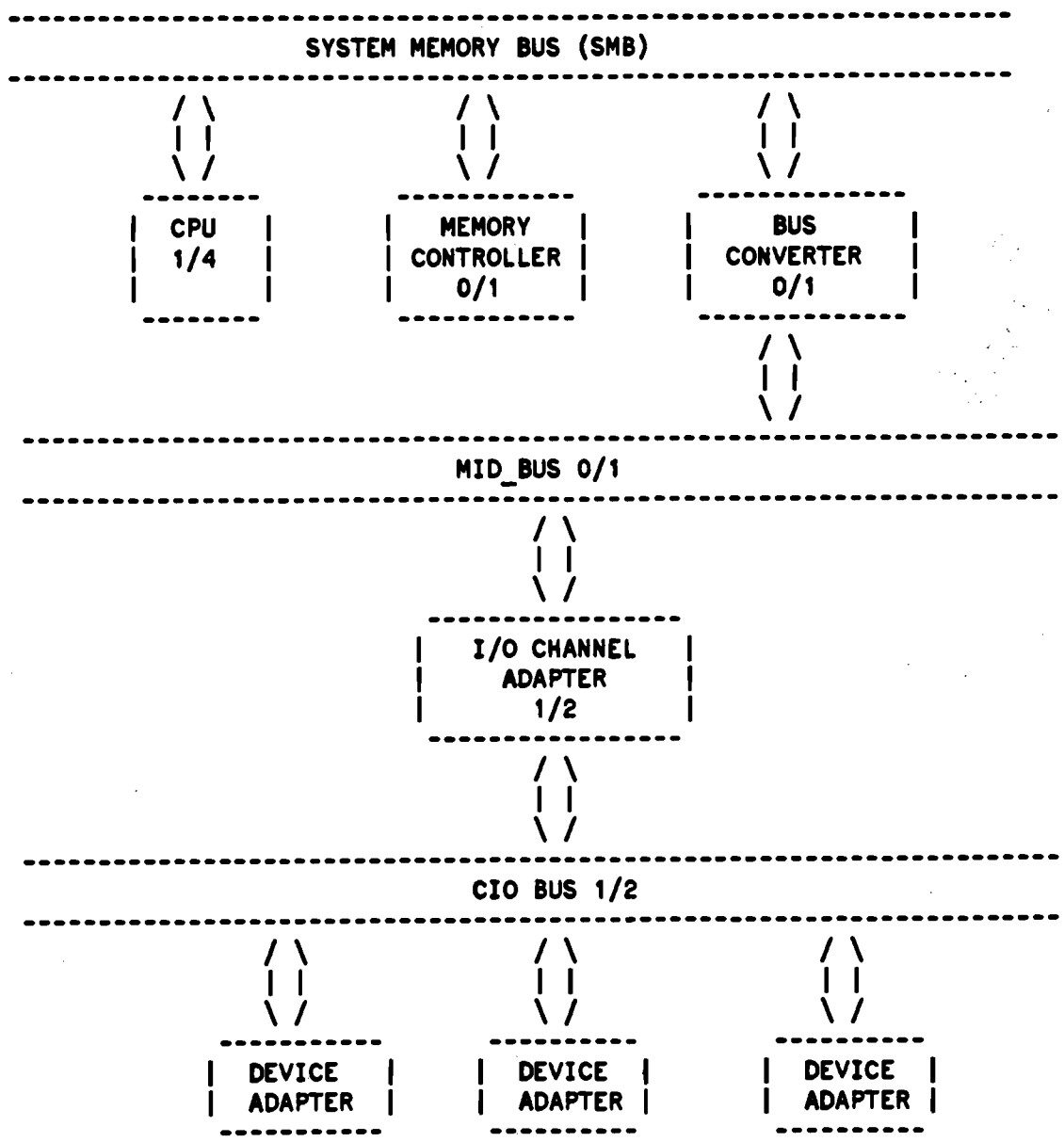
Expansion Module Configured 2 of 8

HP-930 Expansion Bay Configuration Examples

THE HP3000 SERIES 950/955

The 950 Series was HP's follow-on product in the HPPA line. It employed extensive use of VLSI and put the majority of the CPU functions on one board. It also used a single board Channel Adapter and allowed up to 4 of them, for a total of 4 independent CIO Busses within a single bay. It performs at 7 HPPA MIPS, almost twice that of the 840/930. Finally, it is architected to support up to 4 processors for true multi-processor capability although only one is supported today.

The 950 pathing convention does not follow exactly that of the 930. There is an additional upper level bus, called a System Memory Bus (SMB), above the Mid_Bus. Thus, there is an additional path descriptor called a Bus Converter # to contend with. The Bus Converter is another single board VLSI-based device used to interface between the SMB and the Mid_Bus. To date, there can be a maximum of two Bus Converters on a Series 950 system and each Bus Converter can support up to two Channel Adapters. Thus, up to four CIO Busses can be configured as mentioned above. The new set-up looks something like this...



Keep in mind this diagram shows only one CIO Bus. In an attempt to clarify which CIO Bus is associated with which Channel Adapter which is in turn associated with which Bus Converter, the following nomenclature is used...

"CIO X_Y Bus" where X = either 0 or 1 and signifies which Bus Converter (or Mid_Bus) is being used while Y = either 1 or 2 and specifies which Channel Adapter (or CIO Bus) is being used. Thus, the first CIO Bus would be called CIO 0_1 Bus, the 2nd would be called CIO 0_2 Bus, the 3rd would be CIO 1_1 Bus and the 4th would be CIO 1_2 Bus.

The first Bus Converter is assigned an address of 2 and the 2nd Bus Converter is given an address of 6. These addresses are not based on the slot numbers which the Bus Converter cards are plugged into. The Channel Adapter addresses, however, ARE slot number dependent as are the Device Adapter addresses. Let us look at a representation of the I/O backplane of a 950 system for clarification. First notice there are spaces for 2 Mid_Busses and four CIO Busses on this backplane. Notice also the two Mid_Busses are not numbered in the same direction and the CIO Busses each have 5 slots numbered 0 to 4 (they are all numbered in the same direction). The generic path descriptor on the 950 CPU is of the form ...

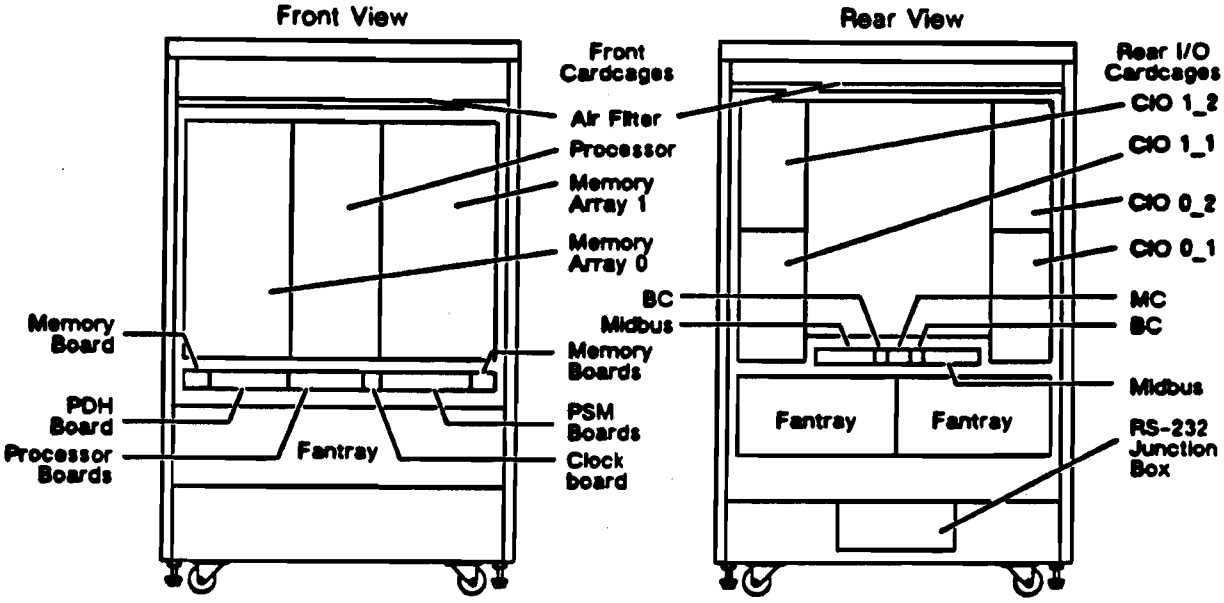
Bus Converter # / IO Channel Adapter # . Device Adapter #. Device #

As already stated, the Bus Converter numbers are either 2 or 6. The Channel Adapter numbers will be either 4 or 8, again depending upon whether the Channel Adapter card is plugged into slot 1 or 2 of the appropriate Mid_Bus. Remember, the formula 4 * Mid_Bus slot # still applies here. The Device Adapter # and the Device # are calculated as before. Thus, there will be four possible groupings of path descriptors which roughly correspond to the appropriate "quadrant" into which the Device Adapters are inserted. They are ...

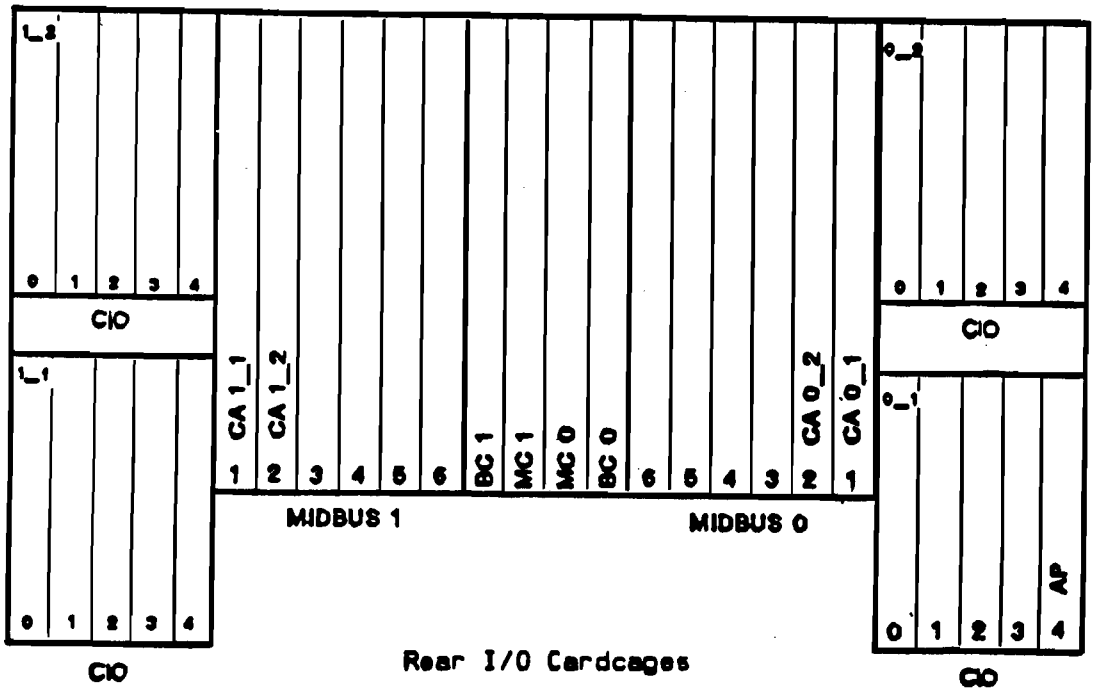
```
2 / 4 . Device Adapter# . Device#  for CIO Bus 0_1  -> lower right hand side
2 / 8 . Device Adapter# . Device#  for CIO Bus 0_2  -> upper right hand side
6 / 4 . Device Adapter# . Device#  for CIO Bus 1_1  -> lower left hand side
6 / 8 . Device Adapter# . Device#  for CIO Bus 1_2  -> upper left hand side
```

An example would be the path for the 1st disc drive which is typically configured as HPIB address 0 on the HPIB Device Adapter plugged into slot 0 of CIO Bus 0_1 (Channel Adapter 1 on Bus Converter 0). Its path would be defined as 2/4.0.0.

The S955 processor is a hardware upgrade to the S950 processor and consists of an entirely new CPU board and Processor Dependent Code (PDC firmware). It is designed to perform at a CPU speed of 11 HPPA and it will allow support of the 2nd memory controller which can provide an additional 128 Mbytes of main memory, for an eventual maximum of 256 Mbytes per system. As such, there were no changes to the I/O architecture or any of the pathing conventions described previously for the S950. For the purpose of this Application Note the two machines can be considered identical.



Processor Bay - Front and Rear Views (Doors Removed)



Rear I/O Cardcages

Model 950

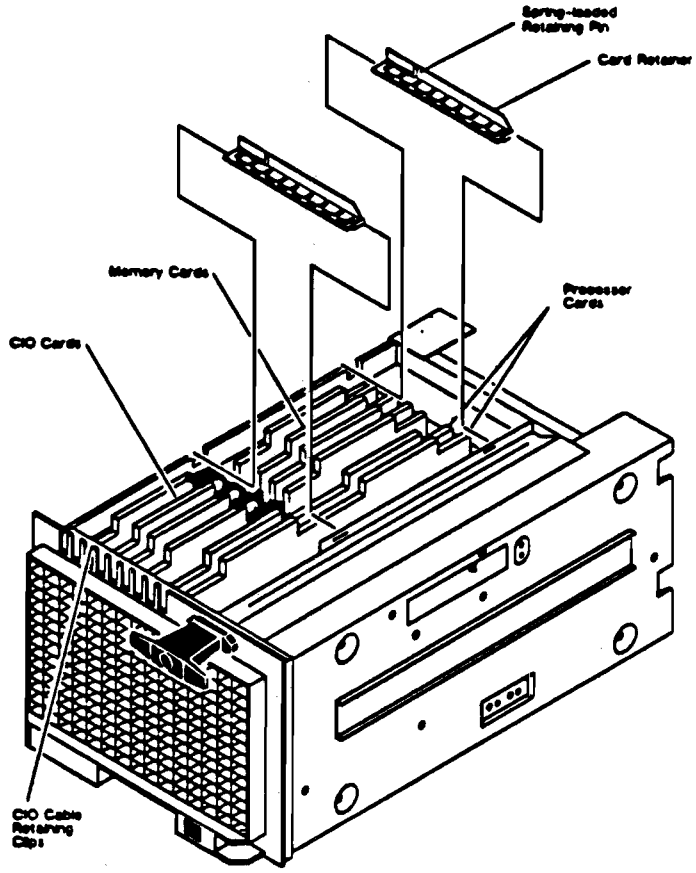
THE HP3000 SERIES 925

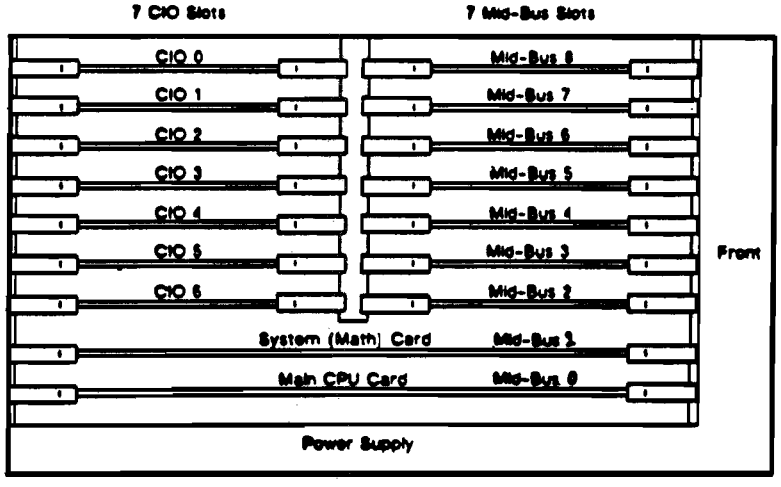
Third in a continuing series of hardware is the Series 925. It employs the same VLSI circuitry used in the Series 950 but in a "shrunk-down" package. Because of this new packaging concept, the non-CIO printed circuit cards were redesigned and changed in both size and functionality. As a result, the I/O paths are somewhat different than the previous two machines. It follows the same pathing conventions as the other HPPA machines and, once the differences in card cage layouts are understood, the I/O path structure becomes apparent. Also, the bus structure is very similar to the Series 930 in that there is only one Mid_Bus and a maximum of two Channel Adapters to deal with. Thus, reference to the bus structure drawings of the 930 given previously should suffice if any clarification is necessary.

Let us begin with the major differences of concern to us in understanding the I/O paths on this CPU series. The 925 CPU, like the Series 930, can come in two different configurations. The main difference being whether of not the optional I/O expander is installed. With no I/O expander, the main CPU card cage will contain only one Channel Adapter and, thus, one CIO Bus. The next figure shows what the card cage for a Series 925 would look like in this instance. Let us take a closer look at this figure. First, note the entire CPU now consists of two cards, a "Main CPU" card and a "System" card. Also, the Mid_Bus slots are located in the front of the cabinet and are numbered 0 to 8. The first Channel Adapter is included on the System card and, since it is in Mid_Bus slot 1, its address is 4 (remember the general formula 4 * Mid_Bus slot #). The CIO card cage slots are in the rear of the cabinet and are numbered in the opposite direction from the Mid_Bus slots. As the drawing shows, there is room for seven CIO cards in the CPU cage which are numbered 0 thru 6. Thus, the address of a CIO card inserted in slot 0 of this cage would be 4.0 and would need to be expanded to 4.0.0 if it was the path leading to an HPIB device with an address of 0.

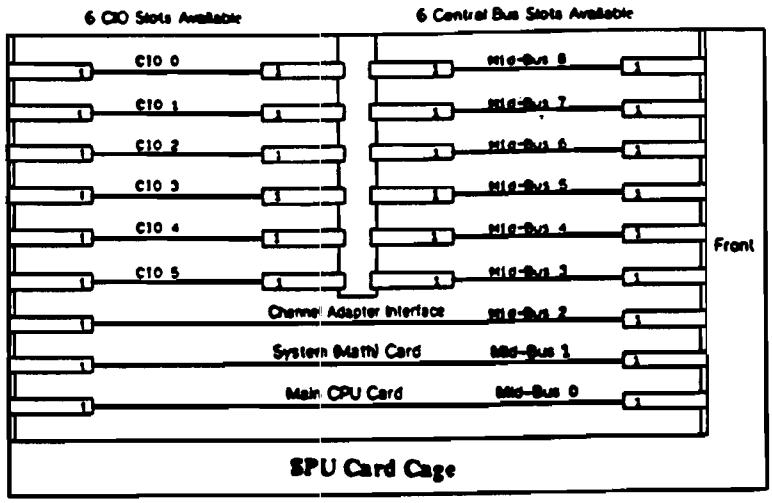
The last figure shows the Series 925 with the optional I/O Expander attached. For configurations with the optional I/O expander there are two Channel Adapters and two corresponding CIO busses. The second Channel Adapter is wholly contained on a card that plugs into Mid_Bus slot 2 in the main CPU cage and attaches to the expander through a CIO Buffer card exactly like in the Series 930. Thus, the address of this second Channel Adapter is 8 (4 * slot #2). Note the inclusion of the 2nd Channel Adapter, in effect, took up one CIO slot as well as one Mid-Bus slot. As a result, there is room for only 6 CIO cards in the main cage - numbered 0 thru 5.

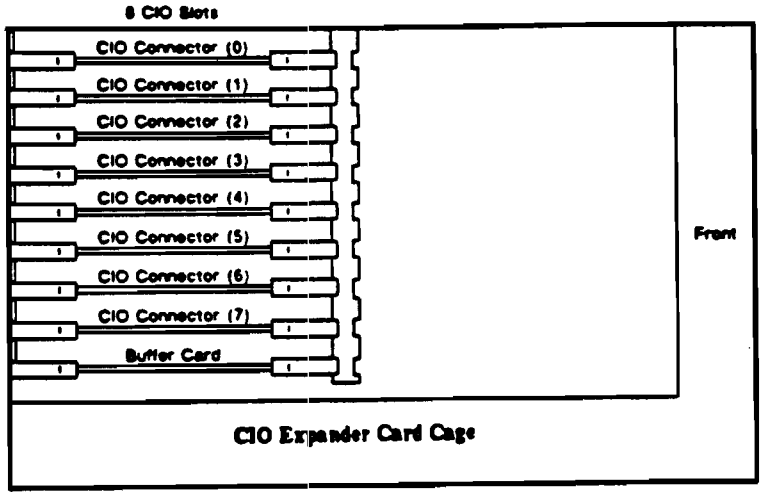
The I/O expander is functionally a separate piece of hardware with self-contained power supplies and other support circuitry. Internally, it contains an additional 8 CIO slots and a special slot for the Buffer Card as shown. The organization of the CIO card cage slots in the expander is the same as in the main CPU cage and they are numbered 0 to 7. It is sometimes helpful to remember whenever you are looking into the rear of either the main CPU cage or the expander, the CIO card positions and their addresses - are numbered from left to right and begin with 0.

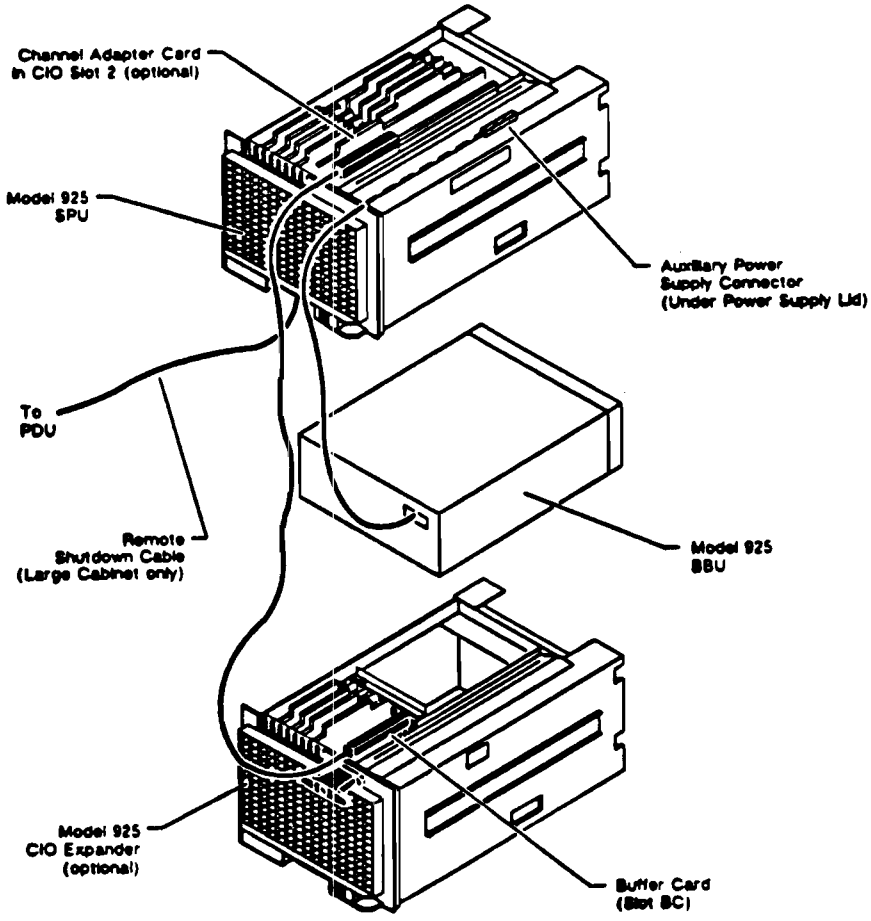

Spring-loaded Retaining Pin
Card Retainer
Memory Cards
Processor Cards
CIO Cards
CIO Cable Retaining Clips


7 CIO Slots
7 Mid-Bus Slots
CIO 0
CIO 1
CIO 2
CIO 3
CIO 4
CIO 5
CIO 6
Mid-Bus 8
Mid-Bus 7
Mid-Bus 6
Mid-Bus 5
Mid-Bus 4
Mid-Bus 3
Mid-Bus 2
System (Math) Card
Mid-Bus 1
Main CPU Card
Mid-Bus 0
Front
Power Supply

Model 925







Model 925 CIO Expander

FOLD FOLD

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FOLD FOLD